UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/670,299	09/26/2003	Toshiaki Minami	03500.017682.	5354

5514 7590 05/05/2006

FITZPATRICK CELLA HARPER & SCINTO
30 ROCKEFELLER PLAZA
NEW YORK, NY 10112

EXAMINER	
WALTER, CRAIG E	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 05/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/670,299	MINAMI, TOSHIAKI	
	Examiner	Art Unit	
	Craig E. Walter	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 9-11* is/are rejected.

7)☒ Claim(s) *8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

1. Claims 1-11 are pending in the Application.

Claims 1, 4-5 and 8-10 have been amended.

Claims 1-7 and 9-11 are rejected.

Claim 8 is objected to.

Response to Amendment

2. Applicant's amendments and arguments filed on 24 March 2006 in response to the office action mailed on 21 October 2005 have been fully considered, but are moot in view of the new ground(s) of rejection necessitated by the change in scope of the newly amended claims.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 3, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peters et al. (US Patent 6,636,927 B1) hereinafter Peters, and in further view of Wu (US Patent 6,970,978 B1).

As for claim 1, Peters teaches a memory control apparatus which performs a reading operation on a memory device at a request of a plurality of masters, comprising (referring to Fig. 2, the memory control unit (element 206) consists of a plurality of masters (elements 224, 222, 226) – col. 6, lines 31-33):

read means for pre-reading data subsequent to data which any of the plurality of masters requests to read (col. 3, lines 35-41 – The bridge device contains prefetch control registers and a prefetch buffer which stores prefetched data for the master devices);

a prefetch buffer for holding a result of the pre-reading (prefetch buffer is shown in Fig. 3, element 304 - col. 6, lines 55-56);

set means for setting a specific master among the plurality of masters (master devices arbitrate for access to the bus, the one which wins arbitration is deemed the initiator - col. 6, lines 36-49 – note in col. 8, lines 53-56 the initiator is called the selected device (i.e. the one 'set') for access to the bus);

Though Peters teaches storing a result of the pre-reading in the prefetch buffer if its determined that the set master issued the request, he fails to teach refraining from changing the content of said prefetch buffer when it is determined that the present master is not specific master as previously set as claimed by Applicant.

Wu however teaches a system and method for providing a pre-fetch memory controller in a computer comprising a plurality of master agents. In his disclosure, the controller is comprised of a plurality of pre-fetch queues, and each master is uniquely

assigned to its own pre-fetch queue (col. 2, lines 1-11). In addition to the static pre-fetch queue assignment as described above, Wu teaches a dynamic assignment of pre-fetch queues to each of the plurality of masters (col. 2, lines 28-31). Using the dynamic assignment approach, Wu teaches assigning pre-fetch queues on an "as-needed" basis. In other words, the assignment occurs once the master has initiated a request to read (and pre-fetch) data. Wu's system allows for any master to make a read request, however only the master responsible for making the request to read data is able to modify data within its own pre-fetch queue. In other words, once the system determines which master is initiating the request, it will only allow that particular master is able to modify the contents of its own pre-fetch queue. A non-limiting example could include master 1 initially requesting a read operation. After the read operation (and subsequent pre-fetch operation), master 2 initiates a read operation. Once the system determines which master (i.e. master 2) initiated the request, the system will read data and pre-fetch data into the queue of the master that made the request (i.e. master 2), thereby refraining from changing the contents of the pre-fetch queue of master 1.

It would have been obvious for Peters to further include Wu's system for providing a pre-fetch memory controller into his bridge device for transferring data. By doing so, Peters would have be able to exploit the benefits of enabling multiple masters to make requests to the system, even after one in particular is selected, while still maintaining coherent pre-fetch data with the use of statically and dynamically assigned pre-fetch queues. Additionally, Peters would benefit from Wu's teachings by mitigating

the risk of unnecessary pre-fetch requests required by the system, hence resulting in considerable bandwidth conservation as taught by Wu in col. 1, lines 56-67.

As for claim 3, Peters teaches the memory control apparatus according to claim 1, wherein said apparatus is connected to the plurality of masters through a shared bus (Fig. 2, element 218).

As for claim 7, Peters teaches the memory control apparatus according to claim 1, wherein said prefetch buffer stores one or more sets of information including data, an address of the data, and a flag indicating the validity of the data (col. 9 lines 10-12 - the requested data is stored in the prefetch buffer – i.e. storing data). The Examiner interprets a "set of information" as a "data" set, an "address of the data" set, or a "flag" set. Since Peters teaches storing a "data" set, his teachings meet the limitations of the claim "one or more" of the aforementioned sets of information.

4. Claims 2 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Peters (US Patent 6,636,927 B1) and Wu (US Patent 6,970,978 B1) as applied to claim 1 above, and in further view of Schelling (US PG Publication 2003/0233492 A1).

As for claim 2, though Peters teaches setting a master from among a plurality of masters through an arbitration process, he does not specifically teach that process as setting the master arbitrarily.

Schelling however discloses a processor selection method for use in multiprocessor systems, and further illustrates that the process of arbitrarily selecting a single processor is well known (paragraph 0008, lines 10-14).

As for claim 11, though Peters teaches setting a master from among a plurality of masters through an arbitration process, he does not specifically teach setting a plurality of specific masters.

Schelling however teaches modifying his selection method to include selecting a group of processors from a plurality of processors (paragraph 0041, lines 1-5).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Peters to further incorporate Schelling's method of selecting a processor or processors, further resulting in maximizing system performance by granting a processor (or plurality of processors) access only if they have the highest health values as taught by Schelling in paragraph 0041, lines 5-12. Schelling assigns health values based on attributes that directly affect the performance of the processors such as execution speed or case temperature of the device – paragraph 0034, lines 1-5 - therefore the overall performance of Peters' system would improve by selecting the processor(s) with best overall performance.

5. Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Peters (US Patent 6,636,927 B1) and Wu (US Patent 6,970,978 B1) as applied to claim 1 above, and in further view of Kamanaka et al. (hereinafter Kamanaka) US Patent 5,522,055.

As for claim 4, the combined teachings of Peters and Wu fail to disclose the apparatus of claim 1, wherein the read means simultaneously pre-reads data

and reads the data requested by the master. Kamanaka however teaches an electronic file system with pre read memory management of data wherein a one master (terminal) is selected from a plurality of masters (col. 20, lines 34-40). The selected master issues a read command to store pre-read data into cache memory (col. 20, lines 48-51). Referring to Fig. 36, data requested by the master and pre-read data are read simultaneously as claimed by applicant as illustrated at in the drawing. The circles refer to a pre-read page (col. 21 – line 18-19) and the triangles designate pages read out of the cache (col. 21, lines 5-17). At time = 1 sec (for terminal 403A) page 5 is being read out (as denoted by the triangle) and page 1 is being pre-read (as denoted by the circle) within the same instant (time = 1 sec).

As for claim 5, the combined teachings of Peters and Wu fail to disclose the apparatus of claim 1, wherein read means as simultaneously reading data requested by the master and pre-reading data subsequent to the requested data. Kamanaka however teaches this limitation. Referring again to Fig. 36, at time = 13 sec, page 13 is being read out of the cache at the same time page 1 is being pre-read subsequent to the requested data, as page 1 is again read at the next subsequent time interval (i.e. pre-read data is read subsequent to the read data).

As for claim 6, the combined teachings of Peters and Wu fail to disclose the apparatus of claim 5, wherein the prefetch buffer stores data requested by the master and data subsequent to the requested data. Kamanaka however

teaches storing the read and pre-read data in a prefetch memory (col. 22, lines 5-7).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate Kamanaka's system which allows for simultaneously reading of pre-read and read data requested by the master into the system of Peter's. By doing so, Peters would improve the access speed (by accessing data in parallel) of his system, which would be beneficial for accessing files of increased size as taught by Kamanaka (col. 1, lines 15-20).

6. Claims 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Peters (US Patent 6,636,927 B1) and Wu (US Patent 6,970,978 B1) as applied to claim 1 above, and in further view of Mekhiel US Patent 6,587,920 B2.

As for claim 9, the combined teachings of Peters and Wu fail to disclose teach comparing a requested address to the address stored in the buffer, and changing a flag to null when the addresses match each other.

Mekhiel however teaches a method for reducing latency in a memory system where a comparator is used to compare a requested address (during a read or write data operation – col. 8, lines 7) to an address stored in a buffer – col. 8, lines 40-45. Mekhiel further teaches the use of a flag bit, which is either set (i.e. dirty) or not set (nullified) if the data is not dirty (i.e. clean) – col. 5, lines 15-22. This way the system can track which data can be replaced after comparing the address of the request and the address in the buffer itself.

As for claim 10, the combined teachings of Peters and Wu fail to disclose comparing a requested address to the address stored in the buffer, and replacing data stored in said prefetch buffer is with data to be written when the addresses match each other.

Mekhiel however teaches a method for reducing latency in a memory system where a comparator is used to compare a requested address (during a read or write data operation – col. 8, lines 7) to an address stored in a buffer – col. 8, lines 40-45. In addition, the flag bit as described by Mekhiel is used to determine "clean" or "dirty" data in the buffer, hence able to replace data to be written as claimed by applicant.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Peters to further include Mekhiel's method of comparing addresses, and maintaining a flag bit to track "dirty" and "clean" addresses. By doing so, Peters would benefit by exploiting the advantages of using Mekhiel's highly associative cache buffer, which compares addresses of the request to the address in the buffer itself (col. 8, lines 40-45). By using this highly associative cache buffer system, Peters would greatly improve the hit rate during read operations as taught by Mekhiel (col. 3, lines 23-27 – higher associatively increases cache hit rate).

Response to Arguments

7. Applicant's arguments with respect to claim 1 have been considered but are moot in view of the new ground(s) of rejection as discussed *supra*. Applicant's assertion that the claims depending on claim 1 are allowable for further limiting an allowable claim is rendered moot, as claim 1 presently stands rejected under 35 USC § 103(a).

Allowable Subject Matter

8. Claim 8 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is an examiner's statement of reasons for allowance:

> Though the combined teachings of Wu and Hooks meet all the limitations of 7, they fail to teach, alone or in combination, wherein when the master requests a read, said control means compares a requested address with an address of data stored in said prefetch buffer, checks a flag of the data, returns the data as read data of the master when the addresses match each other, and stores a result of the pre-read in said prefetch buffer when there is no matching data, and the master is set by the specific master as claimed by Applicant.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Hooks et al. (US Patent 5,761,452), hereinafter Hooks teaches a bus arbiter method and system.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

12. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Craig E Walter
Examiner
Art Unit 2188

CEW

4/27/06

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER